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EXAMINER	
KAWSAR, ABDULLAH AL	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/816,328	LIPPETT, MARK DAVID	
	Examiner	Art Unit	
	ABDULLAH AL KAWSAR	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-61 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/04/2009 has been entered.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

5. Claim 1 recites "a resource management and task allocation controller" wherein the controller is software parse as recited in the claim language lines 3-6 "the controller being in communication with each of the processor elements but separate from the master processing unit, and comprising control logic to allocate executable transactions within the multicore processor to a one of the processor" as the control logic is being used to allocate transactions to the processors without being stored on a storage device or including any hardware with the controller.

Applicant is suggested to amend the claim to incorporate hardware with the controller or storing the control logic on a storage device and executing the control logic by a processor to perform the logical task of the controller.

6. Claims 2-20 do not cure the deficiency of claim 1, therefore they are rejected under the same rational as of claim 1 above.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following claim languages are not clearly understood and indefinite:

i. Claim 1, lines 1-8 recites "a resource management and task allocation controller for a multicore processor having a plurality of interconnected processor elements, each element providing resources for processing executable transactions, the controller being in communication with each of the processor elements but separate from the master processing unit, and comprising control logic to allocate executable transactions within the multicore processor to a one of the processor elements in accordance with one of a range of pre-defined allocation parameters" it is unclear which statue the claim is directed to (i.e. a method

claim? A product claim? Machine claim? A resource management and task allocation controller comprising:?).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-5, 7-14, 18-19, 21-32, 38-41, 47-48, 50, 51, 53 and 56-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bayer et al.(Bayer) US Patent No. 5202987, in view of Barth et al(Barth) US Patent No. 5504670.

11. As per claim 1, Bayer teaches the invention substantially as claimed including a resource management and task allocation controller for a multicore processor having a plurality of interconnected processor elements, each element providing resources for processing executable transactions, the controller being in communication with each of the processor elements but separate from the master processing unit, and comprising control logic to allocate executable transactions within the multicore processor to a one of the processor elements in accordance with one of a range of pre-defined allocation parameters (col 4, lines 18-40).

Bayer does not specifically disclose at least one of which is a master processing unit.

However Barth teaches at least one of which is a master processing unit (col 2, lines 25-29).

12. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Barth into the method of Bayer to have a master processing unit. The modification would have been obvious because one of the ordinary skills of the art would want to have a master processing unit to be able to manage the other processing units with efficient job allocation and resource requirement with proper priority.

13. As per claim 2, Bayer teaches the range of predefined allocation parameters included within the control logic of the controller contains a plurality of transaction scheduling rules, for scheduling the timing and/or order of execution of the executable transactions by the processor elements (col 5, lines 29-44).

14. As per claim 3, Bayer teaches the range of predefined allocation parameters included within the control logic of the controller contains a plurality of system management rules, for controlling the manner in which the executable transactions are executed by the processor elements (col 5, lines 29-44).

15. As per claim 4, Bayer teaches configured to generate instructions for communication to the processing elements (col 7, lines 28-33).

16. As per claim 5, Barth teaches configured to send a processor element configuration instruction to a processor element, which causes the said processor element in turn to be adapted

so as to permit subsequent execution of an executable transaction allocated to that processor element by the controller (col 4, lines 1-9).

17. As per claim 7, Bayer teaches said control logic further comprises:

an executable transaction manager (col 4, lines 29-33); and;

a dedicated memory manager (col 4, lines 58-63);

wherein the said dedicated memory manager controls access by the executable transaction manager to the dedicated memory (col 7, lines 14-18).

18. As per claim 8, Bayer teaches the executable transaction manager further comprises an executable transaction input manager, configured to maintain an indication of available memory within the dedicated memory (col 7, lines 16-22).

19. As per claim 9, Bayer teaches the executable transaction manager input is configured to maintain a list of available memory locations within the dedicated memory (col 4, lines 58-57; col 5, lines 24-31).

20. As per claim 10, Bayer teaches the executable transaction input manager maintains the indication of available memory as a result of updated instructions from the dedicated memory manager (col 4, lines 63-68 through col 5; lines 1-3; lines 9-14).

21. As per claim 11, Bayer teaches the executable transaction to be allocated include threads, each of which form part of an application being executed upon the multicore processor, wherein at least some of the threads are independent threads capable of execution independently of other events, and wherein at least some of the threads are dependent threads, whose execution is dependent upon the existence of a predetermined event (col 5, lines 4-23).

22. As per claim 12, Bayer teaches the control logic further comprises a time manager configured to provide timer functions to said executable transaction manager (col 8, lines 60-68 through col 9, lines 1-3).

23. As per claim 13, Bayer teaches the predetermined event is a timing event (col 5, lines 14-17; lines 29-39).

24. As per claim 14, Bayer teaches the predetermined event is the completion of the execution of a previous thread (col 5, lines 14-17).

25. As per claim 18, Bayer teaches the control logic further comprises a system interface manager, in communication with the executable transaction manager, and configured to manage access by the controller to the multicore processor (col 10, lines 62-67).

26. As per claim 19, Bayer teaches the system interface manager is arranged to provide interconnect interfacing and configuration and run-time access to said executable transaction manager (col 10, lines 65-68 through col 11, lines 1-3).

27. As per claim 21, Bayer teaches the invention substantially including a multicore processor comprising:

a plurality of interconnected processor elements, each element providing resources for processing executable transactions(figure 4);

a resource management and task allocation controller, in communication with each of the processor elements but separate from the processing unit, and comprising control logic for allocating executable transactions within the multicore processor to a one of the processor elements in accordance with one of a range of pre-defined allocation parameters(col 4, lines 18-40); and

Bayer does not specifically disclose at least one of which is a master processing unit;

a plurality of controller clients, at least one of which is associated with a corresponding one of the plurality of interconnected processor elements, wherein each controller client is configured to control communications between its said associated processing element and the rest of the multicore processor, dependent upon control signals from the task allocation controller.

However Barth teaches at least one of which is a master processing unit(col 2, lines 25-29),

a plurality of controller clients, at least one of which is associated with a corresponding one of the plurality of interconnected processor elements, wherein each controller client is configured to control communications between its said associated processing element and the rest of the multicore processor, dependent upon control signals from the task allocation controller (col 4, lines 34-38; col 5, lines 3-7).

28. As per claim 22, Barth teaches a shared system bus accessible by both the controller and the plurality of interconnected processor elements (figure 4, element 410).

29. As per claim 23, Barth teaches an external interface, for connecting said multicore processor to one or more external devices (figure 1).

30. As per claim 24, Bayer teaches a dedicated memory in communication with the controller (col 4, lines 58-63).

31. As per claim 25, Bayer teaches the dedicated memory is exclusively accessible by the controller (col 4, lines 58-60).

32. As per claim 26, Bayer teaches the dedicated memory is accessible by both the controller and by at least one further component of the multicore processor (figure 7, "external access"; col 10, lines 29-49).

33. As per claim 27, Bayer teaches the dedicated memory comprises a plurality of individual memory elements (col 12, lines 49-63).

34. As per claim 28, Barth teaches the number of individual memory elements is user definable (col 4, lines 1-24).

35. As per claim 29, Barth teaches each memory element is of a similar size and the user definable number of memory elements results in a variable memory size (col 7, lines 21-37).

36. As per claim 30, Barth teaches the, or at least one of the controller clients is a software application running on the associated processor element(col 4, lines 1-9).

37. As per claim 31, Barth teaches the, or at least one of the controller clients is a hardware controller client, dependent on the functionality of the associated processor element (col 4, lines 1-9).

38. As per claim 32, Barth teaches each controller client further comprises a client control logic, for controlling the associated processor element, upon activation by a control signal from the said controller (col 5, lines 3-5; lines 33-38).

39. As per claim 38, Bayer teaches the invention substantially as claimed including a method of controlling and allocating resources within a multicore processor having a plurality of

processor elements (col 4, lines 18-25), at least one of which is a master processing unit, comprising:

receiving an executable transaction at a resource management and task allocation controller separate from the master processor unit (col 4, lines 29-67).

allocating that executable transaction to a one of the processor elements independently of central processing unit control(col 4, lines 18-40).

Bayer do not specifically disclose at least one of which is a master processing unit; and receiving an executable transaction at a resource management and task allocation controller separate from the master processor unit.

However, Barth teaches at least one of which is a master processing unit (col 2, lines 25-29),

receiving an executable transaction at a resource management and task allocation controller separate from the master processor unit (col 4, lines 34-49).

40. As per claim 39, Bayer teaches directing the executable transaction to a one of the processor elements via a transaction management client (col 4, lines 58-60).

41. As per claim 40, Bayer teaches wherein the transaction management client is a hardware client (col 4, lines 18-33).

42. As per claim 41, Bayer teaches the transaction management client is a software client (col 4, lines 18-33).

43. As per claim 47, Barth teaches creating, executing or deleting an executable transaction for a first transaction management client, with a second transaction management client (col 6, lines 1-25).

44. As per claim 48, Bayer teaches allocating the executable transaction to a one of the processing elements based upon a pre-defined set of scheduling parameters (col 4, lines 58-68 through col 5, lines 1-3).

45. As per claim 50, Bayer teaches monitoring a list of the scheduling parameters for use by the controller (col 4, lines 29-33).

46. As per claim 51, Bayer teaches comprising altering the set of scheduling parameters over time (col 8, lines 36-68 through col 9, lines 1-3).

47. As per claim 53, Bayer teaches allocating the executable transaction to a one of the processing elements on the basis of the requirement to balance processor resources within the multicore processor (col 8, lines 26-29).

48. As per claim 56, Bayer teaches the step of monitoring the list of the scheduling parameters further comprises maintaining a list of pending tasks that are awaiting a predetermined event (col 4, lines 29-33; col 5, lines 14-16).

49. As per claim 57, Bayer teaches the predetermined event is a timer event, a synchronisation event or both (col 5, lines 9-16).

50. As per claim 58, Barth teaches maintaining a plurality of lists of pending tasks, according to mutually exclusive predetermined events (col 2, lines 52-64).

51. As per claim 59, Barth teaches the step of monitoring the list of the scheduling parameters further comprises maintaining a list of dispatched tasks that are awaiting execution on a particular processing resource (col 2, lines 52-64).

52. Claims 6, 20, 33-37, 45, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bayer et al.(Bayer) US Patent No. 5202987, in view of Barth et al(Barth) US Patent No. 5504670, as applied to claims 1, 21, and 38 above, and further in view of Gulick et al.(Gulick) US Patent No. 6314501.

53. As per claim 6, Bayer and Barth do not specifically disclose configured to generate instructions by the transmission of one or more interrupts to the processor elements.

However, Gulick teaches configured to generate instructions by the transmission of one or more interrupts to the processor elements (col 3, lines 6-12).

54. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Gulick into the combined method of Bayer and Barth to generate instruction by the transmission of interrupts to processing elements. The modification would have been obvious because one of the ordinary skills of the art would want to have instructions to interrupt the processor to be able to communicate between the processing elements.

55. As per claim 20, Gulick teaches the control logic further comprises a system interrupt manager, for converting system interrupts in a first format employed within the multicore processor, into controller interrupts in a second, different format, which second format is understandable by the executable transaction manager (col 44, lines 47-67 through col 46, lines 1-13; col 48, lines 56-67 through col 49, lines 1-14; lines 30-35; col 50, lines 41-60; col 58, lines 43-50; col 59, lines 54-67 through col 60, lines 1-5).

56. As per claim 33, Gulick teaches each controller client further comprises a plurality of buffers, for temporary storage of communication messages sent between the said processor element and the rest of the multicore processor (col 10, lines 64-67; col 38, lines 63-67 through col 39, lines 1-5).

57. As per claim 34, Gulick do not specifically disclose the plurality of buffers are first in first out buffers.

58. It would have been obvious to one of the ordinary skill in the art at the time of the invention to have a first in first out buffer to be able to have a fast communication between the processors.

59. As per claim 35, Gulick teaches each controller client further comprises a plurality of memory elements, each configured to store an address (col 6, lines 8-12).

60. As per claim 36, Gulick teaches each controller client further comprises a plurality of comparators, each comparator configured to compare an address generated by the associated processor element with an address stored in a one of the memory elements (col 20, lines 19-25).

61. As per claim 37, Gulick teaches each controller client further comprises a subtractor, configured to subtract an address stored in a one of the memory elements from an address generated by the associated processor element (col 19, lines 64-67 through col 20 lines 1-18).

62. As per claim 45, Gulick teaches at the transaction management client, storing the whole of a communication message from the rest of the multicore processor to the associated processor element (col 38, lines 63-67 through col 39, lines 1-5); and

subsequently passing the whole message to the associated processor element (col 33, lines 48-59).

63. As per claim 46, Gulick teaches at the transaction management client, streaming communication messages from the rest of the multicore processor to the associated processor element (col 10, lines 64-67).

64. Claims 15-17, 42, 52, 55 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bayer et al.(Bayer) US Patent No. 5202987, in view of Barth et al(Barth) US Patent No. 5504670, as applied to claims 1, 21, and 38 above, and further in view of Hirayama(Hirayama) US Patent No. 5592671.

65. As per claim 15, Bayer and Barth do not specifically disclose the executable transaction manager further comprises an executable transaction synchronisation manager, configured to maintain at least one pending queue list within the dedicated memory, indicative of dependent threads awaiting the occurrence of a predetermined event, and at least one timer queue list within the dedicated memory, indicative of threads awaiting a timing event.

However, Hirayama teaches the executable transaction manager further comprises an executable transaction synchronisation manager, configured to maintain at least one pending queue list within the dedicated memory, indicative of dependent threads awaiting the occurrence of a predetermined event, and at least one timer queue list within the dedicated memory, indicative of threads awaiting a timing event (col 2, lines 64-67 through col 3, lines 1-17).

66. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Hirayama into the combined method of Bayer and Barth

to a list of threads waiting in a queue. The modification would have been obvious because one of the ordinary skills of the art would want to have a waiting queue to be able to manage the thread execution request in order with highest priority for better performance and timely execution of waiting transactions.

67. As per claim 16, Hirayama teaches the executable transaction manager further comprises an executable transaction output manager configured to maintain a plurality of dispatch queue structures within the dedicated memory, indicative of the threads awaiting execution on an associated one of the processor elements, and to maintain a plurality of ready queue structures within the dedicated memory, indicative of threads awaiting allocation to a one of the processor elements for execution there (figure 1, element 12; col 2, lines 58-65).

68. As per claim 17, Hirayama teaches the executable transaction manager further comprises an executable transaction schedule manager, configured to provide and maintain scheduling decisions for prioritising the dispatch of threads from within the ready queues to the dispatch queue for each processor element (col 3, lines 18-29).

69. As per claim 42, Hirayama teaches storing a predetermined address within the transaction management client (col 4, lines 30-33).

70. As per claim 52, Hirayama teaches the step of maintaining the list of the scheduling parameters further comprises maintaining a list of ready tasks that may be carried out by one or more of the processor elements (col 2, lines 64-67 through col 3, line 1).

71. As per claim 54, Hirayama teaches preventing the allocation of the executable transaction to a one of the processor elements, when it is determined that it is desirable for that processor element to execute a higher priority task (col 4, lines 6-26).

72. As per claim 55, Hirayama teaches maintaining a list of executable transactions that have not been allocated for longer that a predetermined length of time (col 3, lines 18-29; col 4, lines 40-47).

73. As per claim 60, Hirayama teaches the step of moving a executable transaction awaiting a predetermined event to the dispatch queue, on expiration of a timeout (col 4, lines 40-43).

74. Claims 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bayer et al.(Bayer) US Patent No. 5202987, in view of Barth et al(Barth) US Patent No. 5504670, in view of Hirayama(Hirayama) US Patent No. 5592671, as applied to claim 38 above, and further in view of Gulick et al.(Gulick) US Patent No. 6314501.

75. As per claim 43, Bayer, Barth and Hirayama do not specifically disclose at the transaction management client, subtracting the predetermined address from an address generated by the associated processing element to produce a normalised address.

However, Gulick teaches at the transaction management client, subtracting the predetermined address from an address generated by the associated processing element to produce a normalised address (col 19, lines 64-67 through col 20 lines 1-18).

76. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Gulick into the combined method of Bayer, Barth and Hirayama to subtract predetermined address from the address generated from the processing element . The modification would have been obvious because one of the ordinary skills of the art would want to be able to allocate available memory location from the change since the memory was pre-allocated.

77. As per claim 44, Gulick teaches at the transaction management client, comparing an address generated by the associated processor element with the stored predetermined address (col 20, lines 19-25); and

configuring the processor element dependent on the result of the comparison (col 20, lines 26-30).

78. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bayer et al.(Bayer) US Patent No. 5202987, in view of Barth et al(Barth) US Patent No. 5504670, as applied to claim 38, and further in view of Summer, Jr. et al.(Summer) US Patent No. 4414624.

79. As per claim 49, Bayer do not specifically disclose the set of scheduling parameters is user-definable (col 5, lines 29-44)

However, Summer teaches the set of scheduling parameters is user-definable (col 15, lines 12-27).

80. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Summer into the combined method of Bayer and Barth to have user definable scheduling parameters. The modification would have been obvious because one of the ordinary skills of the art would be motivated to modify the teaching of Bayer to be able to have user definable scheduling parameters for better system management as desirable by the system user.

81. Claim 61 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bayer et al.(Bayer) US Patent No. 5202987, in view of Barth et al(Barth) US Patent No. 5504670, as applied to claim 21, and further in view of Monahan(Monahan) US Patent No. 4001783.

82. As per claim 61, Bayer and Barth do not specifically disclose wherein said resource management and task allocation controller comprises an external interrupt control logic for

processing external interrupts through a priority structure, wherein said external control logic controllably interrupts said plurality of processing elements based on said priority structure.

However Monahan teaches resource management and task allocation controller comprises an external interrupt control logic for processing external interrupts through a priority structure, wherein said external control logic controllably interrupts said plurality of processing elements based on said priority structure (col 2, lines 35-55).

83. It would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Monahan into the combined method of Bayer and Barth to have a priority structure for external priority. The modification would have been obvious because one of the ordinary skills of the art would be motivated to modify the teaching of Bayer and Barth to be able to have priority structure for interrupts including external interrupts to manage the task execution in a priority structure without interrupting tasks with higher priority in process.

Response to Amendment

84. Applicant's arguments filed 03/04/2009 have been fully considered but they are not persuasive.

85. In remarks applicant argues that:

(1) Bayer and Barth fails to teach a multicore processor as claimed and Multiprocessor system is different from multicore processor.

(2) Bayer fails to teach memory is accessible by both the controller and by at least one further component of the multicore processor.

(3) Gulick fails to teach converting system interrupts from one format to a different format which is understandable by a executable transaction manager.

86. Examiner respectfully disagree with the applicant:

i. As to point (1), applicant supports his argument mentioning that multiprocessor is different from a multicore processor mentioning that "For example, Applicant points out that a multicore processor may include multiple processors or processing elements on a single chip or integrated circuit (IC). As a further example, Applicant points out that a multicore processor may include dissimilar processing elements.". Examiner respectfully disagrees with the applicant. The claimed language does not disclose any of the limitations that show the difference between the multi-core processor and a multiprocessor system as the claimed functionality does not make the difference between them. If the applicant wants the examiner to consider the limitations as explained by the applicant, the applicant is suggested to bring those limitations in the claim for consideration. The claimed limitations as presented are taught by the cited reference. Bayer teaches a multi-core system with plurality of interconnected processor elements(processor) having a scheduler/synchronizer(controller) where each processor provides resources for processing executable transaction and where the scheduler/ synchronizer allocates task to each processor (col 4, lines 18-40; figure 1). Barth teaches a multiprocessor (multicore; figure 4; reference 400) system with plurality of

interconnected processor and a controller. One of the plurality of interconnected processor act as master processor to control the other processors (col 2, lines 25-29; figure 4). The rejection is a 103 rejection with Bayer in view Barth. The references were not cited or consider alone to teach all the limitations of claim 1, instead Bayer teaches a multicore processor system with a controller that controls the task scheduling and assignment for all the processors(Bayer; col 4, lines 18-40; figure 1) but does not teach one of these processor being a master processor wherein Barth teaches a multicore processor system wherein one of the processing unit is a master processing unit (Barth; col 2, lines 25-26).

ii As to point (2), Applicant supports his argument mentioning "that the mention of external access does not teach or suggest the object that is using the external access.". Examiner respectfully disagrees with the applicant. The claim limitation is broad does not specify what is defined by the "**further component of the multicore processor**". Examiner interprets the limitation as having a dedicated memory for the controller that is also accessible by the processor. Bayer teaches the controller unit having dedicated memory accessible by the controller and also by the processor for task management (figure 7, "external access"; col 10, lines 29-49).

vii. As to point (3), applicant supports his argument mentioning that Gulick does not teach converting system interrupts into controller interrupt. Examiner respectfully disagrees with the applicant. Gulick teaches having core services software that

accommodates inter-processor communication and creates(convert) signal based on received signals from a sending client to a receiving client. Core services software gathers information form the request sending client and builds(convert) a signal for the receiving client to be able to process the request (col 44, lines 44-67). Gulick also teaches that the interrupts are signals or messages that are transferred from local processor to shared memory location wherein when the messages are transferred they are converted from one format to a different format for the shared memory location and then converted back when those messages are transferred from the shared location to the specific processor in the specific format (col 58, lines 43-50; col 59, lines 54-67 through col 60, lines 1-5) to be able to store and also make the messages understandable by the other components when the message is in the shared location. If the applicant does not agree with the interpretation of the examiner applicant is also requested to cite the portion of the specification that shows the support and details of the limitation as claimed for better understanding of the claim language and the invention.

Conclusion

87. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH AL KAWSAR whose telephone number is (571)270-3169. The examiner can normally be reached on 7:30am to 5:00pm, EST.

88. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai T. An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

89. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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